CURRICULUM VITAE

ASTRIT ADEMAJ

Born on:	14th Jun 1972 in Peja, Kosova
Citizenship:	Austrian
Contact Address	TTTech Computertechnik AG Schönbrunnerstrasse 7, A-1040, Vienna, Austria
Private address:	Brigittenauer Lände 156-158/6/13, A-1200 Vienna, Austria
Phone:	
Mob:	+43 650 611 5286
E-mail:	astrit.ademaj@tttech.com

Education

1978 – 1986	Primary School in Peja, Kosova
1986 – 1990	Gymnasium „11 Maji“ in Peja, Kosova
June 1990	High-school leaving certificate (graded excellent) from Gymnasium „11 Maji“ in Peja. Section: mathematics
1990 – 1995	MSc studies in the Faculty of Electrical Engineering, section of Informatics and Telecommunications University of Prishtina, Prishtina, Kosova
September 1995	Graduation in the Faculty of Electrical Engineering with distinction. Average of grades: 9.05 out of 10.
1997-1998	German Language Learning School “Vorstudienlehrgang”, Vienna, Austria
1998 – 2003	PhD Studies (“Assessment of Error Detection Mechanisms of the Time-Triggered Architecture Using Fault Injection”) and Research Assistant at the Real-Time Systems Group at the Institute for Computer Engineering, Vienna University of Technology, Vienna, Austria.
April 2003	Graduation of the doctoral studies in Computer Science at the Vienna University of Technology with Prof. Hermann Kopetz as research advisor.

Work experience

1995-1997	Software Developer and Computer Course Teacher, in Peja and Deçan, Kosova
1998-2002	Freelance database developer with for different companies in Vienna (concert ticket reservation, project managing and finances, charter-flight ticket reservation, etc.).
1998	Implementation of the C-code for the current version if the TTP/A protocol, in a MC68HC11P/711 controller
2000-2004	Research Assistant at the Technical University of Vienna.
2000-2003	Department group leader in the International European Community Research Project FIT (Fault Injection for Time-Triggered Architecture) - contract number IST-1999-10748. Development of the Software Implemented Fault Injection (SWIFI) and Monitoring tool for Time-Triggered Architecture. Involved in the experiments with heavy-ion radiation (using a Californium-252) in a series of visits at the Chalmers University of Technology in Gothenburg, Sweden.
2000-2003	Validation of the TTP/C protocol using fault injection. Validation of TTA systems with bus and star topology
2003-2004	Involved in the International European Community Research Project Next TTA (High-Confidence Architecture for Distributed Control Applications) - contract number IST-2001-32111.
2004-2008	Assistant Professor at the Technical University of Vienna.
2004-	Guest Lecturer at the University of Prishtina, (in the course of Brain Gain Programme from WUS-Austria) Lectured courses: • *System Programming* • *Computer Architecture*,

- *Real-Time Systems*

2004-2007 Involved in the Integrated Project within the EU Framework Programme 6 DECOS (Dependable Embedded Components and Systems).

2005- Project evaluator for the EUROPEAN COMMISSION-founded research projects in the course of IST (Information Society Technologies) of the 6th Framework Programme (FP6) on "*Safety on Road Transport"* and 7th Framework Programme (FP7) "Intelligent Vehicles".

2008-2010 Guest Lecturer at the Vienna University of Technology,

2008- Product and Project Manager at the TTTech Computertechnik AG in Vienna, Austria.

Experience with

- Programming: assembler Pascal, C, C++, C#, VBA, PHP.
- Microcontrollers: 68HC11P/711 , Motorola 68360, Motorola 68376, MPC555, MPC855, CF5275, Powerquicc II MPC8260.
- MS-SQL, MS Access databases, mySQL.
- OS: Windows, Linux, VxWorks, OSE.
- System programming and embedded system development.
- Project management.

Research Interests:

- Software and Hardware Fault Injection Methods
- Testing, Verification and Validation of Safety-Critical Systems
- Real-Time Systems
- Time-Triggered Communication Systems
- Distributed Fault-Tolerant Systems
- Embedded Systems

Languages

Albanian	Mother tongue.
English	Read, written and spoken **fluently**
German	Read, written and spoken **fluently**
Serbo-Croatian	Read, written and spoken **fluently**

List of Publications

Mirko Jakovljevic and Astrit Ademaj
Ethernet Protocol Services for Critical Embedded Systems Applications.
The 29th IEEE/AIAA Conference on Digital Avionics Systems Conference (DASC), Salt Lake City, UT , USA, 3-7 Oct. 2010, pp 5.B.3-1 - 5.B.3-10

Vaclav Mikolasek, Astrit Ademaj, *Stanislav Racek*
Segmentation of Standard Ethernet Messages in the Time-Triggered Ethernet.
The 13th IEEE conference on the Emerging Technologies and Factory Automation, Hamburg, Germany, September 15-18, 2008.

Astrit Ademaj and Hermann Kopetz.
Time-Triggered Ethernet and IEEE 1588
International IEEE Symposium on Precision Clock Synchronization for Measurement, Control and Communication. Vienna, Austria, October 1-3, 2007.

Astrit Ademaj**.**
Fail-Silent Assumptions in Fault-Tolerant Systems
Journal on *International Review on Computers and Software (I.RE.CO.S.),* Issue Sept. 2007

Jonny Vinter, Henrik Eriksson, Astrit Ademaj, Bernhard Leiner, and Martin Schlager
Experimental Evaluation of the DECOS Fault-Tolerant Communication Layer
To be published at the 26th International Conference on Computer Safety, Reliability and Security (SAFECOMP), , Nuremberg, Germany, September 2007

Marco Serafini, Jonny Vinter, Astrit Ademaj, Fulvio Tagliabò, Jens Koch, Wolfgang Brandstätter and Neeraj Suri
A Tunable Add-On Diagnostic Protocol for Time Triggered Systems
The 37th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), Edinburgh, UK, June, 2007

Klaus Steinhammer and Astrit Ademaj
TT Ethernet controller design.
International Embedded Systems Symposium, San Diego, USA, June 2007.

Astrit Ademaj, Alexander Hanzlik, Hermann Kopetz
Tolerating Arbitrary Failures in a Master-Slave Clock-Rate Correction Mechanism for Time-Triggered Fault-Tolerant Distributed Systems with Atomic Broadcast.
IEEE Real-Time Networks and Systems Conference Nancy, France, March 2007

Hermann Kopetz, Astrit Ademaj, Alexander Hanzlik
Combination of clock-state and clock-rate correction in fault-tolerant distributed systems.
Real-Time Systems Journal, Volume 33, Numbers 1-3, July 2006

David de Andrés, Sara Blanc, Pedro Gil, Astrit Ademaj, Klaus Steinhammer
BUFI: Fault injector for communication buses.
IEEE Conference on Dependable Systems and Networks (DSN06), June, 2006

Petr Grillinger, Astrit Ademaj, Klaus Steinhammer, Hermann Kopetz
Software Implementation of Time-Triggered Ethernet Controller.
Workshop on Factory Communication Systems - WFCS 2006, June, 2006

Astrit Ademaj, Hermann Kopetz, Petr Grillinger, Klaus Steinhammer, Manfred Prammer
Integration of Predictable and Flexible In-Vehicle Communication using Time-Triggered Ethernet.
SAE World Congress, April, 2006 (selected as outstanding technical paper)

Alexander Hanzlik, Astrit Ademaj
A Composable Algorithm for Clock Synchronization in Multi-Cluster Real-Time Systems.
Fourth Workshop on Intelligent Solutions in Embedded Systems - WISES06, Vienna, Austria, June 30th, 2006

Astrit Ademaj, Klaus Steinhammer, Petr Grilliger, Hermann Kopetz, Alexander Hanzlik
Fault-Tolerant Time-Triggered Ethernet Configuration with Star Topology.
Dependability and Fault Tolerance Workshop. March, 2006

Klaus Steinhammer, Petr Grillinger, Astrit Ademaj, Hermann Kopetz
A Time-Triggered Ethernet (TTE) Switch
Design, Automation and Test in Europe, Munich. Germany, March 6-10. 2006

Philipp Peti, Roman Obermaisser, Astrit Ademaj, Hermann Kopetz
A Maintenance-Oriented Fault Model for the DECOS Integrated Diagnostic Architecture
Workshop on Parallel and Distributed Real-Time Systems 2005 (WPDRTS)

Hermann Kopetz, Astrit Ademaj, Petr Grillinger, Klaus Steinhammer
The Time-Triggered Ethernet (TTE) Design
8th IEEE International Symposium on Object-oriented Real-time distributed Computing (ISORC), Seattle, Washington, May, 2005

Hermann Kopetz, Astrit Ademaj, Alexander Hanzlik
Integration of Internal and External Clock Synchronization by the Combination of Clock-State and Clock-Rate Correction in Fault-Tolerant Distributed Systems
The 25th IEEE International Real-Time Systems Symposium, Lisbon, Portugal, Dec. 2004 (selected as one of the best 5 papers in the conference).

Astrit Ademaj.
Achieving Fail Silence in the Time-Triggered Architecture.
In Proceedings of the 6th IEEE International Workshop on Design and Diagnostic of Electronic Circuits and Systems, Poznan, Poland, April 2003.

Astrit Ademaj, Hakan Sivencrona, Günther Bauer, Jan Torin.
Evaluation of Fault Handling of the Time-Triggered Architecture with Bus and Star Topology. In Proceedings of the IEEE International Conference on Dependable Systems and Networks (DSN 2003), *San Francisco, USA, June 2003.*

Astrit Ademaj
A Methodology for Dependability Evaluation of the Time-Triggered Architecture Using Software Implemented Fault Injection.
In Proceedings of the fourth European Dependable Computing Conference, EDCC-4, *Toulouse, France, October 2002.*

Astrit Ademaj.
Slightly-Off-Specification Failures in the Time-Triggered Architecture.
In Proceedings of the 7th Annual IEEE International Workshop on High Level Design Validation and Test, *Cannes, France, October, 2002.*

Idriz Smaili, Astrit Ademaj.
Setting Break-Points in Distributed Time-Triggered Architecture.
In Proceedings of the 7th Annual IEEE International Workshop on High Level Design Validation and Test, *Cannes, France, October, 2002.*

Astrit Ademaj, Pavel Herout, Petr Grillinger, Jan Hlavicka.
Fault Tolerance Evaluation Using two Software Based Fault Injection Methods.
In Proceedings of the IEEE International On-Line Testing Workshop (IOLTW02), *Isle of Bendor, France, July 2002.*

Sara Blanc, Astrit Ademaj, Hakan Sivencrona, Pedro Gil, Jan Torin.
Three Different Fault Injection Techniques Combined to Improve the Detection Efficiency for Time-Triggered Systems.
In proceedings of the 5th IEEE International Design and Diagnostic of Electronic Circuits and Systems Workshop, *Brno, Czech Republic, April 2002.*

Vienna, 11.05.2011

Astrit Ademaj